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MODEL PCI-DA12-2/4/6

USER MANUAL

FILE: MPCI-DA12-6.C3a

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Table of Contents

Chapter 1: Introduction

Features

- 2, 4, or 6 Channels of Analog Output, 12 Bits Resolution.
- 16 Digital I/O Lines Buffered on the Card.
- Digital I/O Buffers Can Be Tri-stated under Program Control.
- Pull-Ups on Digital I/O Lines.
- Resettable fused +5V and +12V supplies available, 0.5A at Room Temperature.

Description

The card is a half-size card that can be installed in any PCI slot of PC-AT class computers. It contains two, four, or six double-buffered digital-to-analog converters (DACs) that provide independent analog output channels of 12-bit resolution. Each analog output channel can be configured for ranges of:

0V to +2.5V
0V to +5V
0V to +10V
-2.5V to +2.5V
-5V to +5V
-10V to +10V
4mA to 20mA

The analog output channels have a double-buffered input for single-step update and each is addressed at its own I/O location. Type AD7237 double-buffered, dual, DAC chips are used. The analog outputs can be updated either independently or simultaneously.

The DAC outputs are undefined at power-up. Therefore, in order to prevent excessive outputs to external circuits, the card contains automatic circuits that set D/A outputs to less than 15 percent of span at system power-on. Upon power-up, the card is in the Simultaneous Update mode. After all DACs have been loaded with the desired values, a software command can be used to switch the reference voltage to its normal value. Similarly, a software command can be used at any time to set the reference voltage to 15 percent causing all DAC outputs to be equal to 15 percent of each DACs programmed value.

Each I/O line is buffered by a type 74ABT245B tristate buffer transceiver capable of sourcing 32 mA or sinking 64mA. Pull-ups on the card assure that there are no erroneous outputs at power up. The lines initialize in the input mode, the buffers are configured by hardware logic for input or output according to direction assignment from a control register in the PPI.

Specifications

Analog Outputs

- Resolution: 12 Binary bits (0 to 4095 decimal)
- Channels: 2, 4, or 6 Voltage output or Current sink channels
- Current Range: 4 to 20 mA (with excitation voltage 8-36 VDC)
- Voltage ranges (5mA max): 0V to +2.5V
  0V to +5V
  0V to +10V
  -2.5V to +2.5V
  -5V to +5V
  -10V to +10V

AD7237 D/A Converter, Double Buffered / Simultaneous Update

- Relative Accuracy: + ½ LSB
- Monotonicity: 12 bits over operating temperature range
- Settling Time: 8 usec to one LSB for full-scale step input
- Linearity: + ½ LSB integral non-linearity over rated temperature range
- Gain Stability: 15 ppm/ °C
- Output Drive Capability: 5mA maximum
- Short-Circuit Current: 25 mA maximum
- Output Resistance: Less than 0.1 Ω
- Data Format: 12-bit binary, right justified, and offset binary for bipolar outputs

Digital I/O

Outputs

- Logic High: 2.0 VDC min., source 32 mA
- Logic Low: 0.55 VDC max., sink 64 mA

Inputs

- Logic High: 2.0 to 5.0 VDC, Input Load: +20 µA
- Logic Low: -0.5 to +0.8 VDC, Input Load: -20 µA

Environmental

- Operating Temperature Range: 0 °C. to +60 °C
- Storage Temperature Range: -20 °C. to +85 °C
- Humidity: 5% to 95% non-condensing

- External DAC Reference (input): +4.5V to +5.5V
- 5V Source (output): 0 to 500 mA, fused (resetting)
- 12V Source (output): 0 to 500 mA, fused (resetting)
- Size: 6" long (152 mm)
- Power Required: +5 VDC at 250 mA typical with all digital outputs at high impedance
  +12 VDC at 116 mA maximum (6 channels)
  -12 VDC at 56 mA maximum

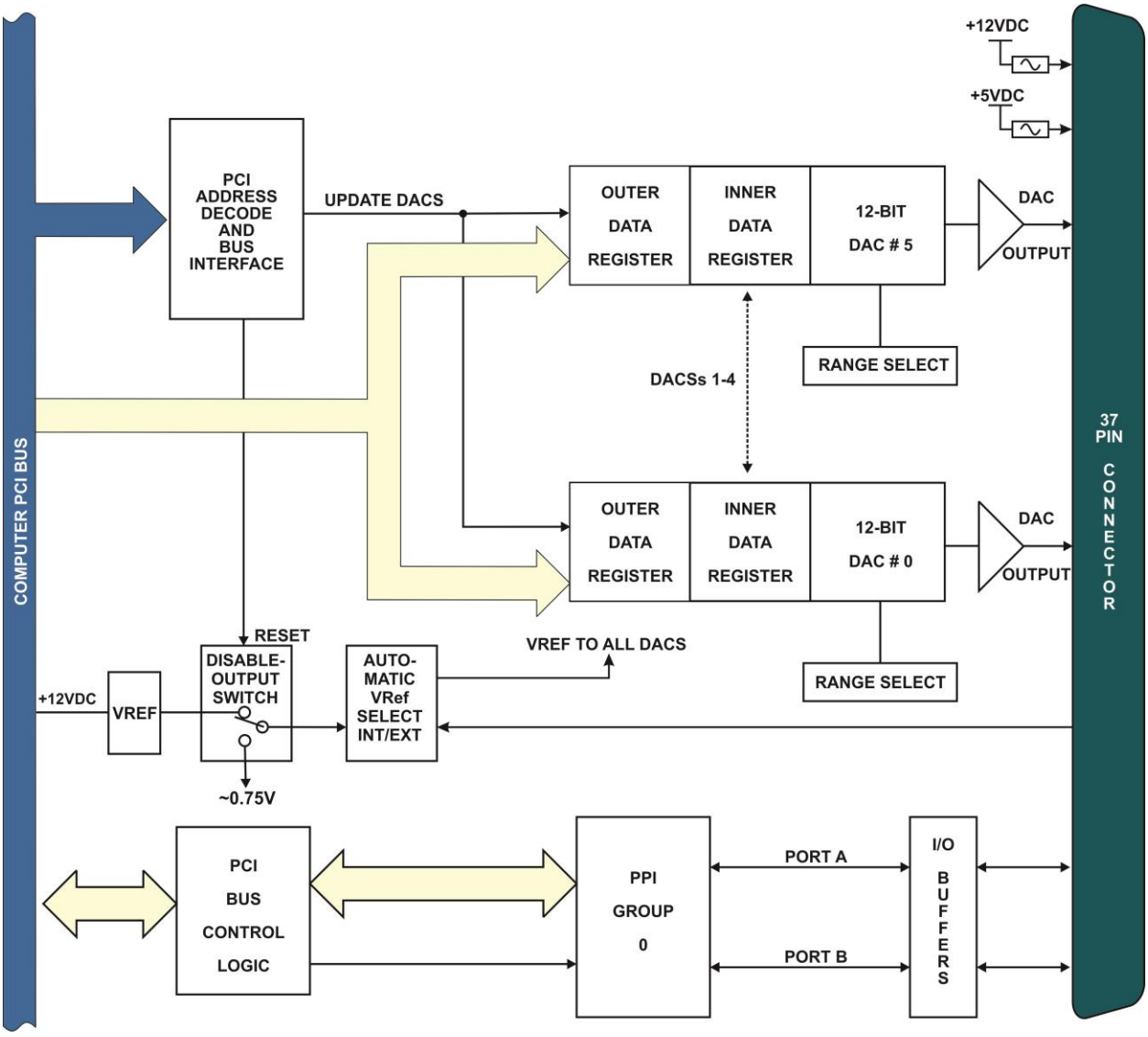


Figure 1-1: Block Diagram

Chapter 2: Installation

The software provided with this board is available by request on CD for a fee, or downloaded via the product page for free and must be installed onto your hard disk prior to use.

Installing from Downloaded Installer

Windows

1. Visit the product web page at http://acces.io/cardname
2. Download the Software Package from the Downloads tab
3. Run the Install program and follow the on-screen prompts to install the software for this board

Linux

1. Please visit http://github.com/accesio for information on installing under Linux.

Installing from CD

Perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your drive where you see D: in the examples below.

Windows

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type d:install, click OK or press K.
3. Follow the on-screen prompts to install the software for this board.

Caution! * ESD ***A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.***

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETUP.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Carefully install the card in an available 5V PCI or Universal PCI-X expansion slot (you may need to remove a backplate first).
6. Inspect for proper fit of the card and tighten screws. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7. Install an I/O cable onto the card's bracket mounted connector.
8. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
9. Run PCIfind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
10. Run one of the provided sample programs that was copied to the newly created card directory (from the CD) to test and validate your installation.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck PCIFind or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In DOS, the PCI\SOURCE directory shows the BIOS calls used to determine the address and IRQ assigned to installed PCI devices. In Windows, the Windows sample programs demonstrate querying the registry entries (created by PCIFind and NTIOPCI.SYS during boot-up) to determine this same information.

Chapter 3: Option Selection

Voltage output ranges are determined by switch settings as described in the following paragraphs. Also, the method to update D/A outputs is programmable as described here and in Chapter 5, Programming .

Output Ranges

There is a three-position slide switch associated with each DAC channel to make voltage range selection: switches S1 (Channel 0) through S6 (Channel 5). A silk-screen diagram on the card defines switch positions to use for each range. In addition to the switch, one jumper per channel is used to select Voltage vs Current Output. The following table presents the same information:

Voltage Range	**Sn-1**	**Sn-2**	**Sn-3**	**OUT 0-5**
0 to +2.5V	OFF	OFF	ON	Set in Position V
0 to +5V	OFF	OFF	OFF	
0 to +10V	OFF	ON	OFF	
-2.5V to +2.5V	ON	OFF	ON	
-5V to +5V	ON	OFF	OFF	
-10V to +10V	ON	ON	OFF	
Current Range	**S1**	**S2**	**S3**	**OUT 0-5**
4 mA to 20 mA	OFF	OFF	OFF	Position I

Analog Output Update

Analog outputs are updated under program control in either one of two ways:

a. Automatic Update: Each channel is updated individually when new data are written to the related high-byte base address. Individual update mode may be set by a special read operation as defined in the programming section of this manual.

OR

b. Simultaneous Update: The outputs of all D/As may be updated simultaneously. This is done by first enabling simultaneous updating for all outputs and then preloading the low and high bytes of each DAC and then initiating a simultaneous update by software command.

Refer to Chapter 5, Programming of this manual for more detail.

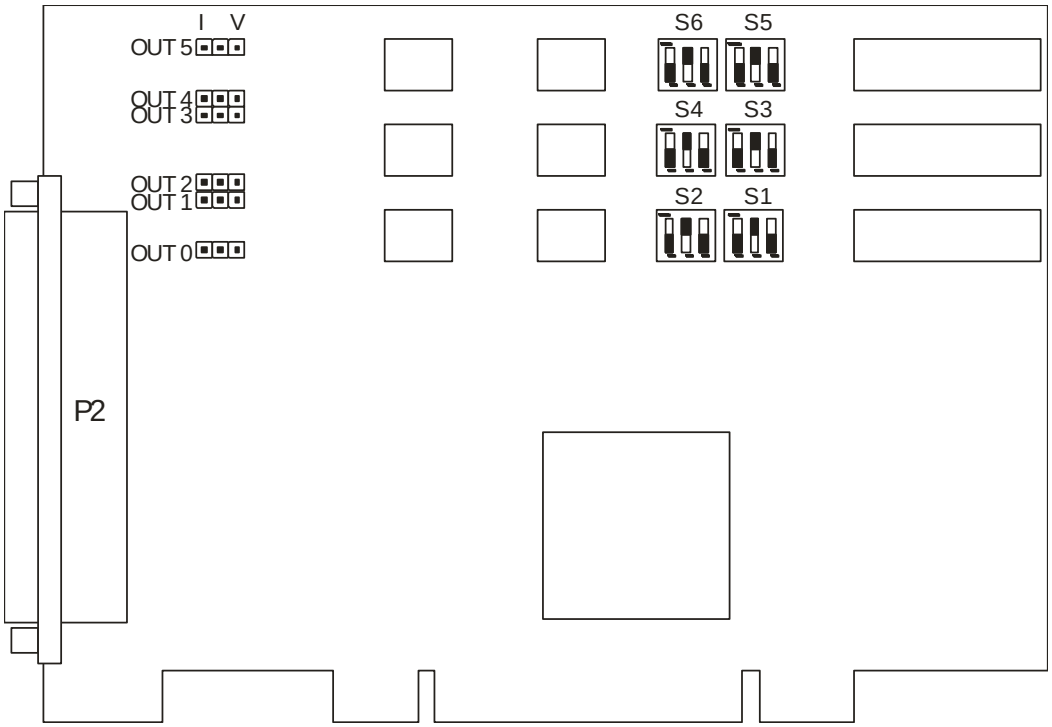


Figure 3-1: Option Selection Map

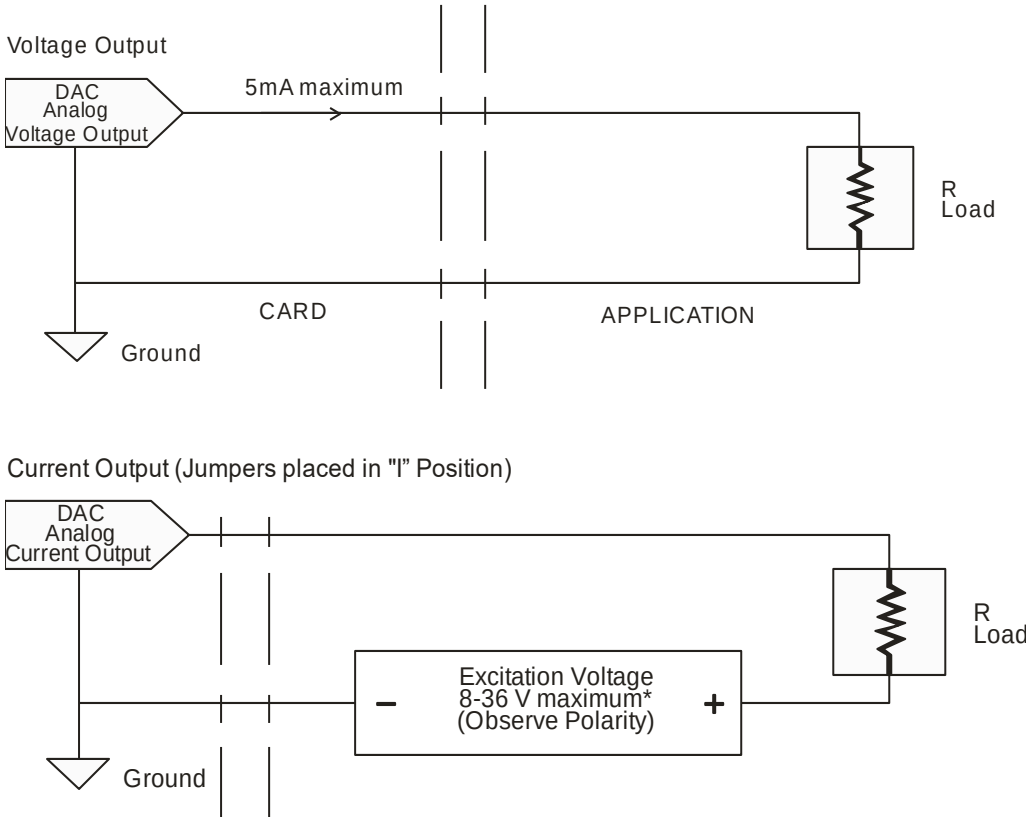


Figure 3-2: Field Wiring

Caution!
Do not connect current loops in a DAC that is set to voltage mode. The loop supply can destroy the DAC.

Chapter 4: Address Selection

These cards use two I/O address spaces, one of 64 bytes and one of 256 bytes. The DACs and control registers occupy the first 16 bytes of the first area. The next 16 addresses are reserved. The digital I/O circuit uses the next 4 register locations. The other 28 addresses are reserved. The 2nd I/O address space of 256 bytes is used for software calibration data. These two I/O address spaces are defined in the Port Address Selection Table in the Programming section of this manual.

PCI architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCI cards, rather than the user. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternately, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

PCIFind uses the Vendor ID and Device ID to search for your card, then reads the base addresses and IRQ.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for these cards is 494F. (ASCII for "IO")

The Device ID for the 2 is 6C90h.
The Device ID for the 4 is 6C98h.
The Device ID for the 6 is 6CA0h.

The control / DAC / I/O base address is BaseAddresses[2] in the PCI_COMMON_CONFIG structure, while the calibration base address is BaseAddresses[3].

Chapter 5: Programming

These cards' DACs and Digital I/O use 40(hex) consecutive I/O addresses. Programming the cards is very straightforward as there are only two operating modes, three range-selection switches per channel, and one unique addition. The basic operation of a Digital-to-Analog card is to write a 12-bit value to a Digital to Analog Converter (DAC) pre-load (outer) register where it is buffered and loaded by an update command to a DAC (inner) register. Outputs of that register control a "ladder" network which produces the analog output. The output voltage range is defined by settings of the range-selection switches for that channel. In C:

```
outport(BASE+(CH*2), (Volts*4096/10)-2048);
```

would output "Volts" volts to channel "ch", assuming a bipolar 5V range. For other bipolar ranges, substitute the appropriate voltage span in place of "10" in the equation. For unipolar ranges, remove the "-2048" and use the appropriate voltage span in place of the "10".

Upon power-up, or hardware reset, the DAC registers are restricted to a safe value and the card is set in Simultaneous Update mode. *Since the pre-load register is not cleared upon power-up, but left at an undefined value, a known value must be written to the preload registers before using a "Clear Restrict-Output-Voltage" command.*

Simultaneous Update Mode is the power-up or default mode of operation for the DAC card. When a value is written to a DAC address the output does not change until an output update is commanded via a read from Base Address +8. (Alternatively, a read of Base Address +A will update the DAC registers and switch the board to Automatic Update Mode.) While in Simultaneous Update Mode, a single read will load all DAC registers with the value waiting in the pre-load registers, causing all outputs to be updated and changed simultaneously.

Automatic Update Mode is the configuration that changes a DAC output immediately after the high-byte of the new value is written to the DAC address. If the card is in Simultaneous Update Mode a read of Base Address+2 will change the card back to Automatic Update Mode without updating the outputs. A read of Base Address +A will update all outputs simultaneously and then place the card in Automatic Update Mode.

Restrict-Output-Voltage limits the output of all DAC channels and is active at power-up. Since the pre-load register is not cleared upon power-up, but left at an undefined value, known values must be written to the preload registers before using a "Clear Restrict-Output-Voltage" command. Those written values will then be output to the connector when a "Clear Restrict-Output-Voltage" command is issued by a read of Base Address +F.

External Trigger Update Mode allows a negative level at pin 25 of the I/O connector to cause the DACs to be updated. A read of Base Address +5 will enable this mode, a read of Base Address +6 will disable it. Note that this pin is shared with the External Interrupt signal.

External Interrupt is a negative edge at pin 25 and is latched until cleared by a read of Base Address +4. The interrupt is enabled by a read of Base Address+3 and powers up disabled. After being cleared the interrupt must be re-enabled.

Address	Write *	Read
Base + 0	DAC 0 Low Byte	Place card in Simultaneous Mode without updating outputs.
Base + 1	DAC 0 High Byte	
Base + 2	DAC 1 Low Byte	Release card from Simultaneous Mode without updating outputs.
Base + 3	DAC 1 High Byte	Enable External Interrupts
Base + 4	DAC 2 Low Byte	Disable External Interrupts
Base + 5	DAC 2 High Byte	Enable External DAC Update
Base + 6	DAC 3 Low Byte	Disable External DAC Update
Base + 7	DAC 3 High Byte	
Base + 8	DAC 4 Low Byte	Update all outputs and place card in Simultaneous Mode.
Base + 9	DAC 4 High Byte	
Base + A	DAC 5 Low Byte	Update all outputs and release card from Simultaneous Mode.
Base + B	DAC 5 High Byte	
Base + C		
Base + D		
Base + E		Restrict-Output-Voltage (Limits outputs to 15% of full scale range).
Base + F		Clear Restrict-Output-Voltage (Allows full operating output voltage).

* Although it is possible to write the low and high bytes separately as shown above, it is much easier to write both bytes with a single OUT DX, AX instruction. In that case, only even addresses are written. In any case, DACs 2 and 3 only exist on the 4/6 model and DACs 4 and 5 only exist on the 6 model.

Table 5-1: Register Map

Address	Write	Read
Base + 20	Digital I/O Port A, Output	Digital I/O Port A, Input
Base + 21	Digital I/O Port B, Output	Digital I/O Port B, Input
Base + 22		
Base + 23	Digital I/O Control Byte	

Table 5-2: I/O Address Map for the Digital I/O

All addresses are in hex.

The Digital I/O Control Byte sets the directions of Port A and Port B.

	Port B Input	Port B Output
Port A Input	92h	90h
Port A Output	82h	80h

Table 5-3: Digital I/O Control Byte Values

BIT	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B7	B6	B5	B4	B3	B2	B1	B0
High Byte	x	x	x	x	B11	B10	B9	B8

Table 5-4: DAC Data Format

For Unipolar ranges: For Unipolar ranges, data are in true binary form.

```
                XXXX  0000  0000  0000   =  Zero
                XXXX  1000  0000  0000   =  ½ Scale
                XXXX  1111  1111  1111   =  Full Scale
                      |                |
MSB or B11      ←                      →   B0 or LSB
```

For Bipolar ranges: For Bipolar ranges, data are in offset binary form.

```
                XXXX  0000  0000  0000   =  -Full Scale
                XXXX  1000  0000  0000   =  Zero
                XXXX  1111  1111  1111   =  +Full Scale
                      |                |
MSB or B11      ←                      →   B0 or LSB
```

Note

PPI Mode 1 cannot be used with this circuit without modification. Thus, bits D2, D5, and D6 should always be set to "0". If your card has been modified to operate in Mode 1, then there is an Addendum sheet in the front of this manual describing that modification. This circuit cannot be modified to operate in PPI Mode.

The circuit is initialized by the computer Reset command (all ports set for input and all buffers enabled). Both the 8255 control register and the buffer direction latch are accessed at the same address.

The 8255 control register will latch a new configuration byte when it's written to with bit D7 high. If, for example, hex 80 is sent to Base Address+23, the group 0 PPI will be configured in mode 0 with ports A, B, and C as outputs.

At the same time, data bit D7 is also latched in the buffer controller. A high state puts the buffers in the tristate mode; i.e., disabled. Now, if any of the ports are to be set as outputs, you may set the values of the respective port with the outputs still in tristate condition. Lastly, to enable the ports a control byte with bit D7 low must be sent to Base Address+23.

Note

All data bits except D7 must be the same for the two control bytes. Those buffers will now remain enabled until another control byte with data bit D7 high is sent to Base Address+23.

Chapter 6: Software

These cards are straightforward to program. The following example is in C, but sample code is also provided for use in DOS in C, and Pascal, and four Windows languages: C#, Delphi, VBasic, and VisualC.

To output an analog value with 12-bit resolution, a corresponding decimal number N between 0 and 4095 is calculated ($2^{12} = 4096$).

N/4096 = V(out)/V(full scale)

Next the data are written to the selected analog output channel. (See the preceding I/O Address Map.) In this example, we will assume analog output on channel zero (AO 0).

outport (BASE + 0, N)

For simplicity, it was assumed that the simultaneous-update capability was not used.

Examples of this routine are found on the sample disk along with examples in other languages.

Chapter 7: Calibration

Periodic calibration of the cards is recommended if they are used in extreme environmental conditions. The card uses very stable components but high-low temperature cycles might result in slight analog output errors.

This card is calibrated by software using the following formula:

$$Y= (4096 -a - b)/4096) * X + b$$

To calibrate the card, run the calibration program and follow the screen prompts. No attempt at calibration should be made in noisy locations or with a noisy calibration setup.

The calibration program stores various data to the card to facilitate calibrating the data output in a run-time environment. The data collected during calibration is stored in an EEPROM located at the second of the I/O base addresses assigned to the device (BaseAddresses[3] in the PCI_COMMON_CONFIG structure). The EEPROM contains two values per channel per range. The ZERO (or OFFSET) and the SPAN calibration constants are stored (a and b from the equation above) for each channel at each possible range (0-6). These constants are used during normal operation to calibrate the output data in real-time. Refer to the samples provided on disk for an example of using this data.

In addition to 'a' and 'b' as shown above, the EEPROM contains a table of ranges assigned to each channel. Starting at Base+F0, 6 base addresses contain one byte each, from 0-6, indicating the voltage output range assigned to that channel. It is important to use the calibration program at least once if the default range (+/- 10V) is changed on any channel, to allow this table of data to be reconfigured. If this data is incorrect, calibration is not guaranteed.

Word Address	Range	Offset ('b' in formula)	Span ('a' in formula)
Base + 00h to Base + 0Ah	0 to +5 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + 20h to Base + 2Ah	0 to +2.5 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + 40h to Base + 4Ah	0 to +10 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + 60h to Base + 6Ah	-5 V to +5 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + 80h to Base + 8Ah	-2.5 V to 2.5 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + A0h to Base + AAh	-10 V to 10 V.	DAC 0 to DAC 5	DAC 0 to DAC 5
Base + C0h to Base + CAh	4 to 20 mA.	DAC 0 to DAC 5	DAC 0 to DAC 5

The next table shows the location of the range data for each channel. The value stored is a number from 0 to 6, representing the 7 ranges (as shown in the table below). If you set any channel's range switch, be sure to place the correct value in this table. Using the calibration program provided is generally the easiest method of ensuring the table remains accurate.

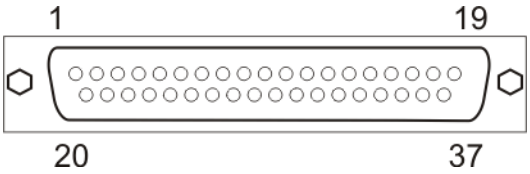
Byte Address	Channel
Base + F0h	Channel 0
Base + F1h	Channel 1
Base + F2h	Channel 2
Base + F3h	Channel 3
Base + F4h	Channel 4
Base + F5h	Channel 5

Value	Range
0	0 - 5V
1	0 - 2.5V
2	0 - 10V
3	-5 - +5V
4	-2.5 - +2.5V
5	-10 - +10V
6	4 to 20mA

Note that the **analog reference voltage** (available on the connector at pin 29) is 5.1V. This is 2% higher than the typical value of 5V to allow room for calibration. If the software calibration feature isn't needed, the user can apply 5V at pin 28 to be used as the DAC reference.

Chapter 8: Connector Pin Assignments

The analog outputs are accessible via a male 37-pin D type connector.



Pin	Function	Pin	Function
1	Analog DAC 5 Output	20	Ground
2	Analog DAC 4 Output	21	Ground
3	Digital I/O Port B - Bit 7	22	Ground
4	Digital I/O Port B - Bit 6	23	Ground
5	Digital I/O Port B - Bit 5	24	Ground
6	Digital I/O Port B - Bit 4	25	External Interrupt / DAC Update
7	Digital I/O Port B - Bit 3	26	+5V, fused
8	Digital I/O Port B - Bit 2	27	+12V, fused
9	Digital I/O Port B - Bit 1	28	Analog Reference, Input
10	Digital I/O Port B - Bit 0	29	Analog Reference, Output
11	Ground	30	Digital I/O Port A - Bit 7
12	Analog DAC 3 Output	31	Digital I/O Port A - Bit 6
13	Ground	32	Digital I/O Port A - Bit 5
14	Analog DAC 2 Output	33	Digital I/O Port A - Bit 4
15	Ground	34	Digital I/O Port A - Bit 3
16	Analog DAC 1 Output	35	Digital I/O Port A - Bit 2
17	Ground	36	Digital I/O Port A - Bit 1
18	Analog DAC 0 Output	37	Digital I/O Port A - Bit 0
19	Ground		

Table 8-1: P2 Connector Pin Assignments

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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